Lógica Reconfigurável

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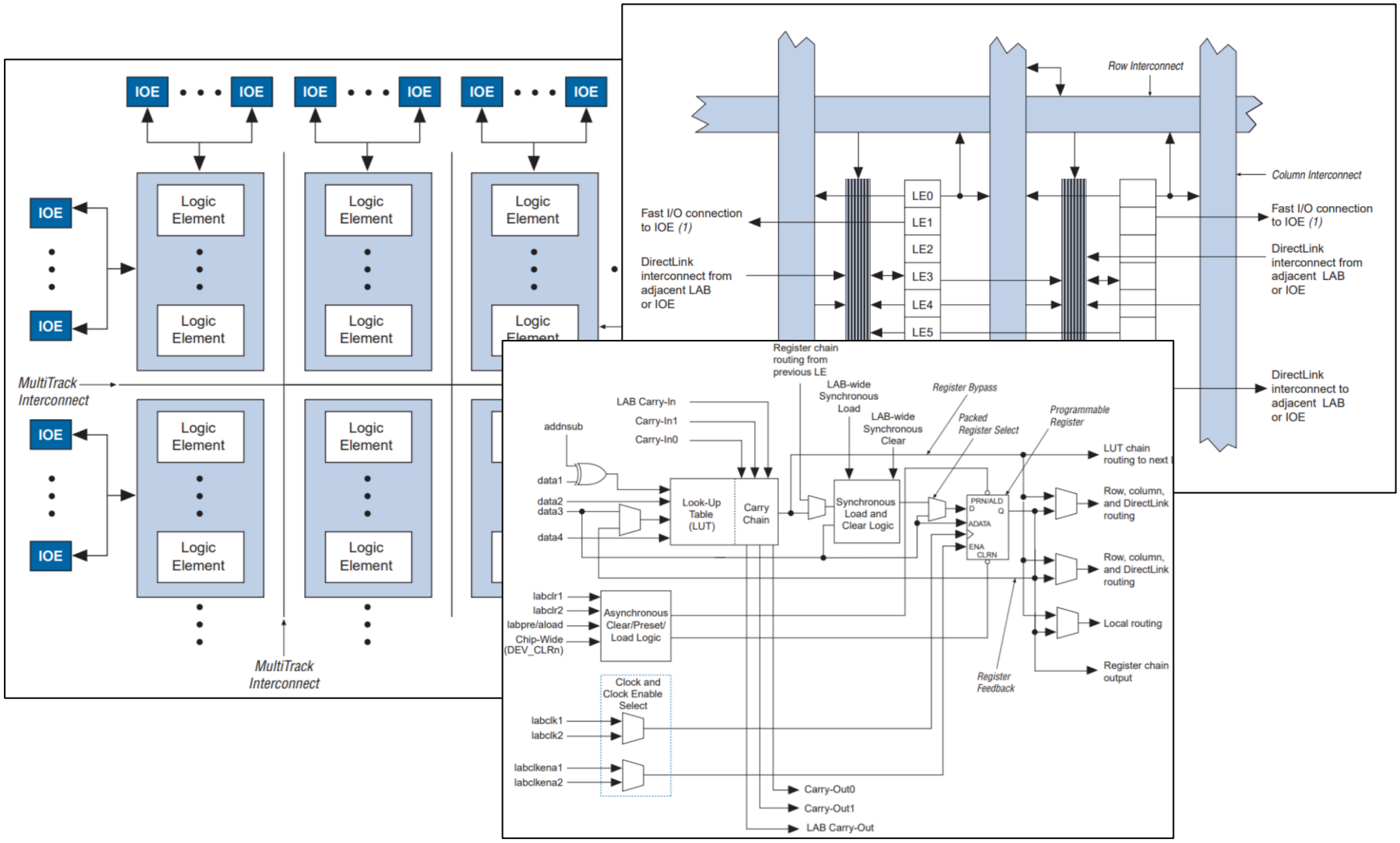
https://ricardokers.github.io/

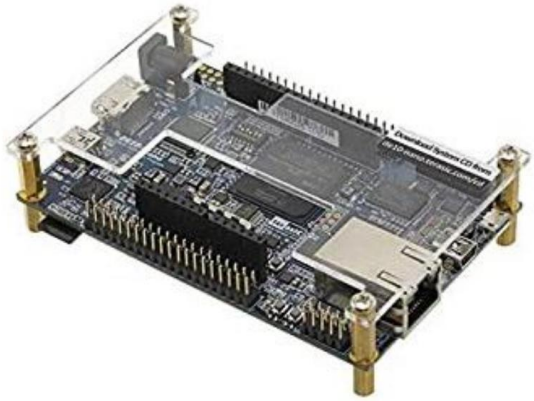
Ementa

Fundamentos de lógica reconfigurável



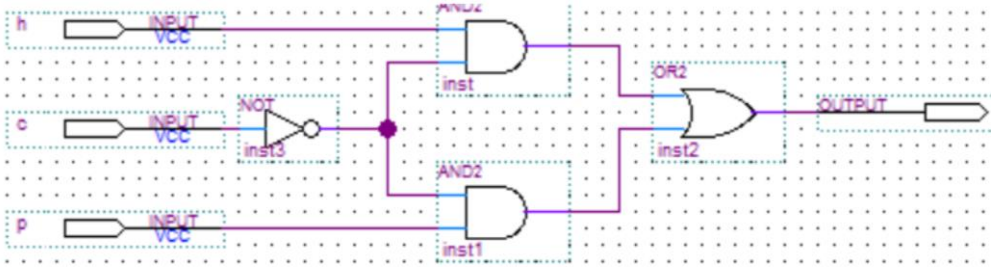
Ementa

Estudo dos dispositivos lógicos reconfiguráveis.

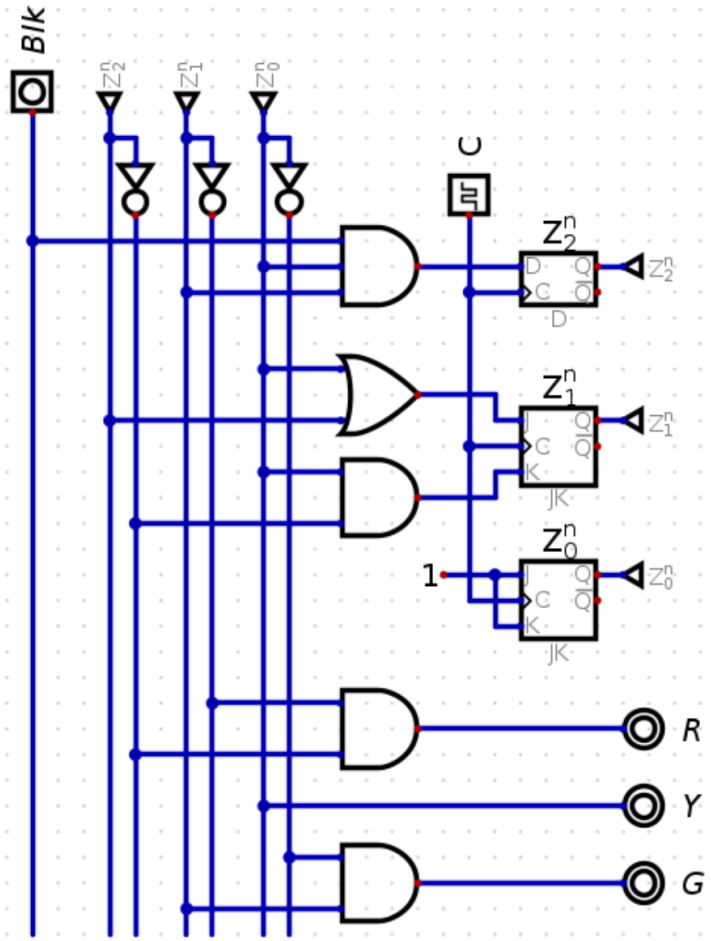


Ementa

Estudo de uma linguagem para síntese de circuitos em dispositivos lógicos reconfiguráveis.

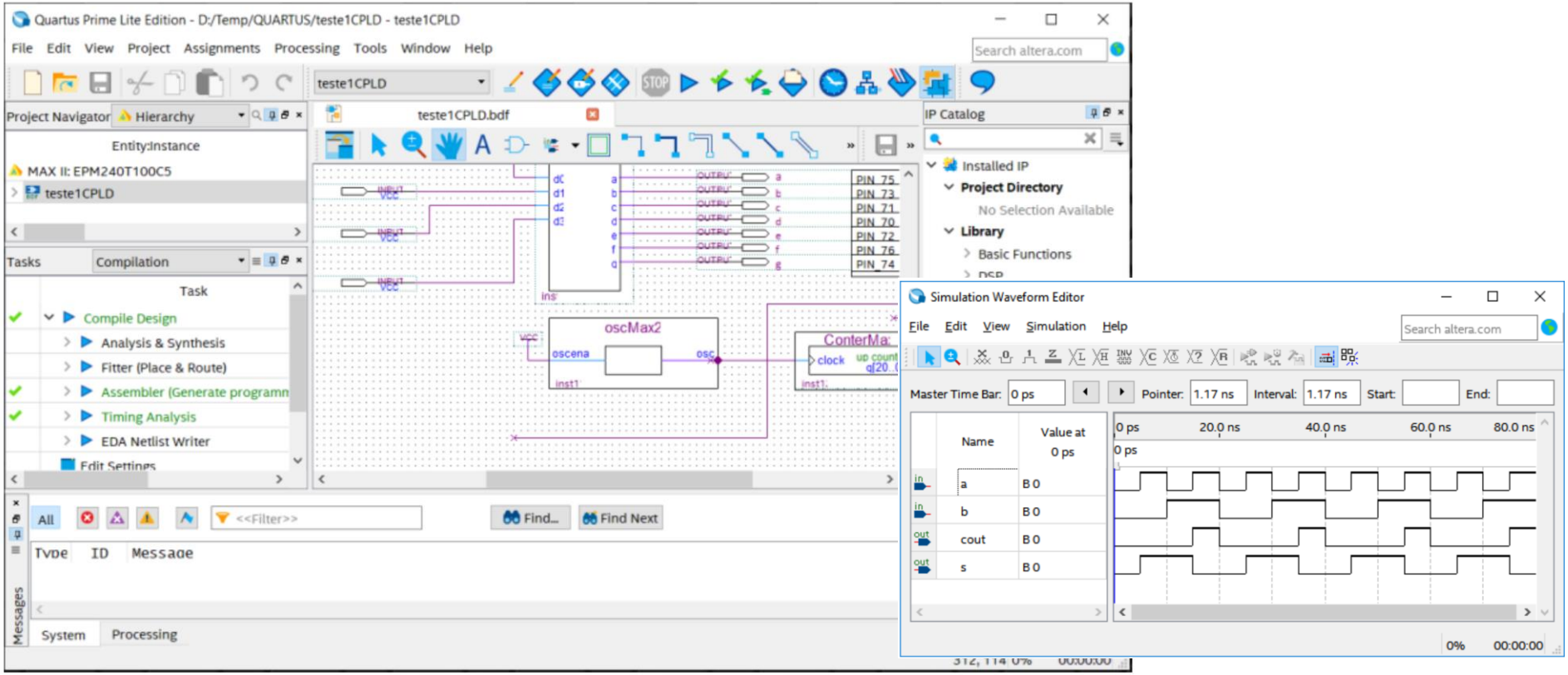



```
library ieee;
use ieee.std_logic_1164.all;

entity Driver7SegMAX2 is

   port
   (
      d0 : in std_logic;
      d1 : in std_logic;
      d2 : in std_logic;
      d3 : in std_logic;

      a  : out std_logic;
      b  : out std_logic;
      c  : out std_logic;
      d  : out std_logic;
      e  : out std_logic;
      f  : out std_logic;
      g  : out std_logic
   );

end entity;
```



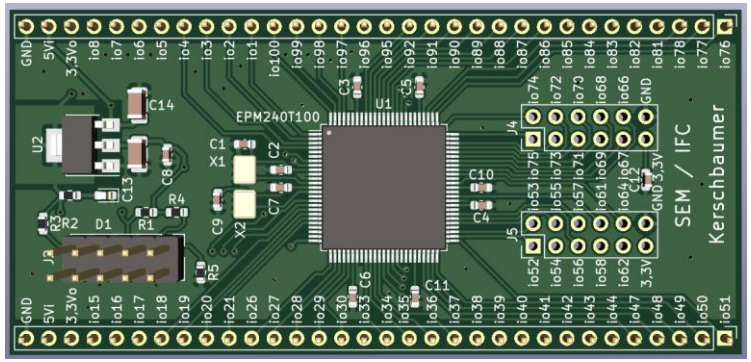
Ementa

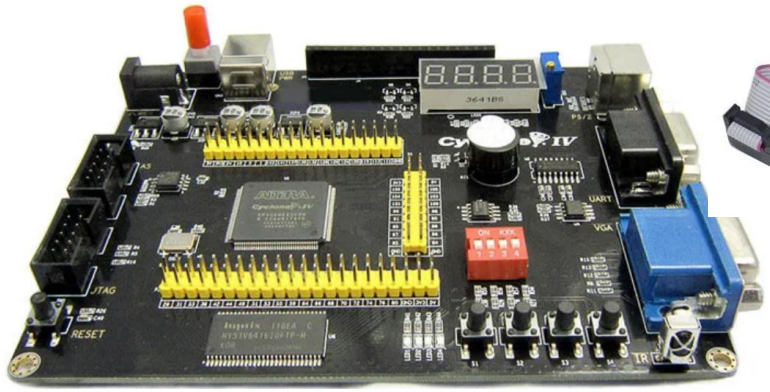
Estudo de ferramentas de EDA (Electronic Design Automation) para o desenvolvimento automatizado de projetos e simulações de circuitos em lógica reconfigurável

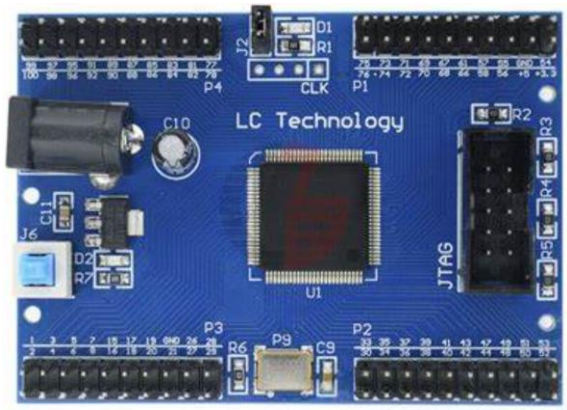


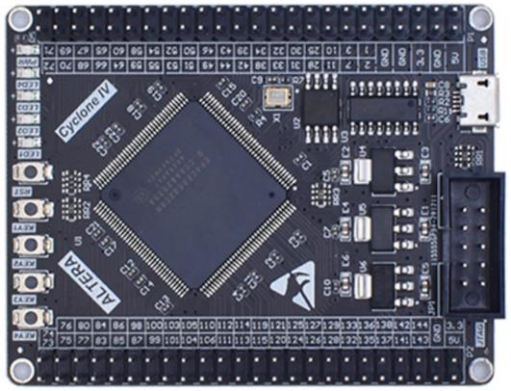
Ementa

Desenvolvimento de projetos de circuitos digitais em lógica reconfigurável utilizando diagramas de blocos, linguagem de síntese e máquinas de estados.

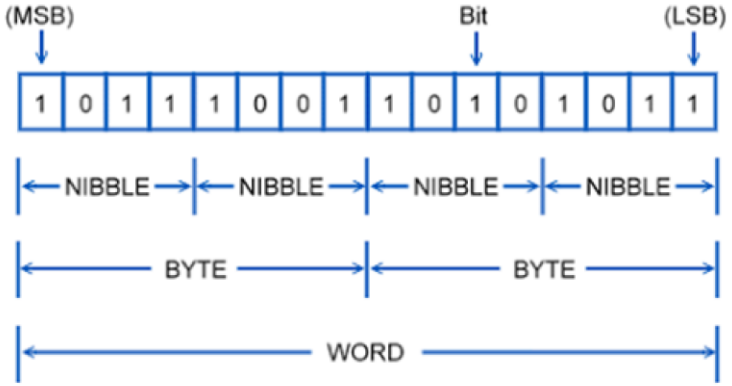








Revisão

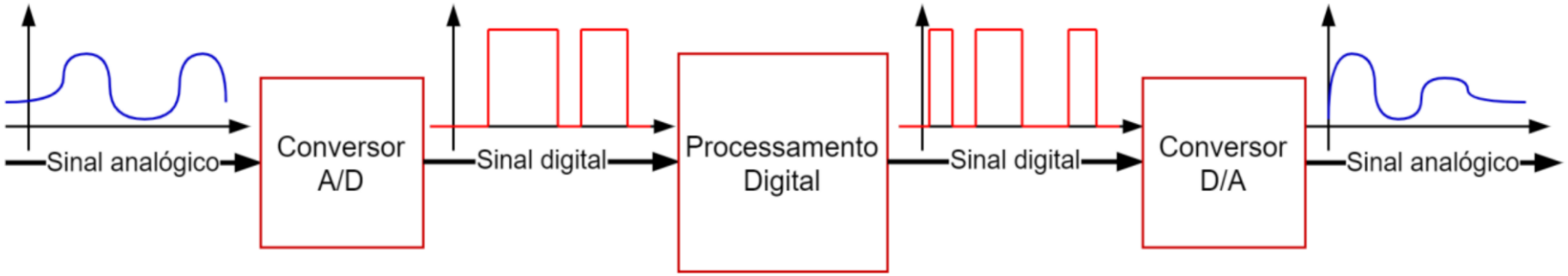


		Sinal	Magnitude			
11_{10}	=	**0**	1	0	1	1
-11_{10}	=	**1**	0	1	0	1
9_{10}	=	**0**	1	0	0	1
-9_{10}	=	**1**	0	1	1	1

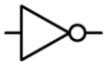
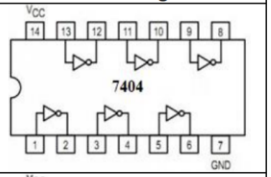
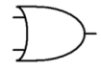
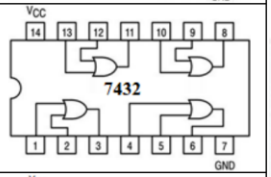
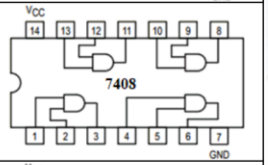
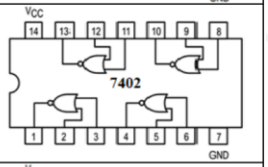
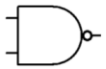
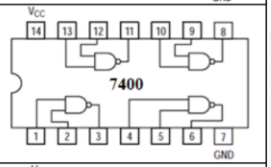
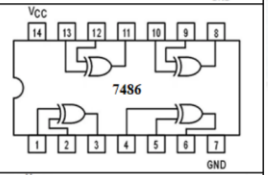
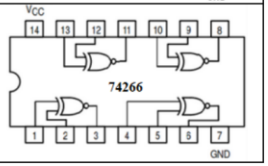
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	…	2^{-22}	2^{-23}

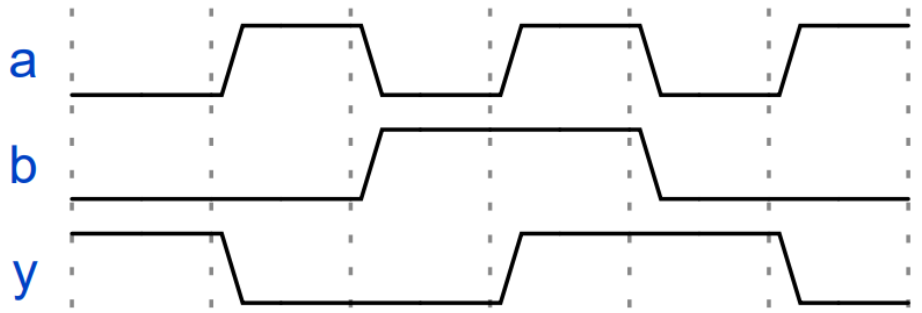
S	Expoente (E)	Parte fracionária (F)
1 bit	8 bits	23 bits

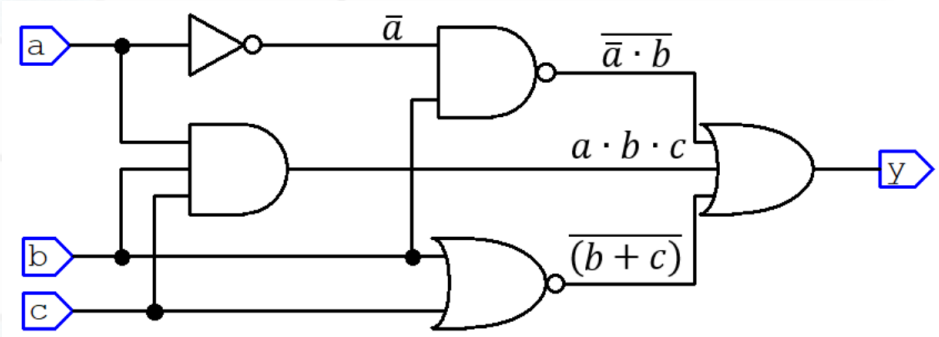
Decimal	Binário	Octal	Hexa
0	0	0	0
1	1	1	1
2	1 0	2	2
3	1 1	3	3
4	1 0 0	4	4
5	1 0 1	5	5
6	1 1 0	6	6
7	1 1 1	7	7
8	1 0 0 0	1 0	8
9	1 0 0 1	1 1	9
10	1 0 1 0	1 2	A
11	1 0 1 1	1 3	B
12	1 1 0 0	1 4	C
13	1 1 0 1	1 5	D
14	1 1 1 0	1 6	E
15	1 1 1 1	1 7	F
16	1 0 0 0 0	2 0	1 0
17	1 0 0 0 1	2 1	1 1
18	1 0 0 1 0	2 2	1 2
19	1 0 0 1 1	2 3	1 3
20	1 0 1 0 0	2 4	1 4
Pesos →	16 8 4 2 1	8 1	16 1

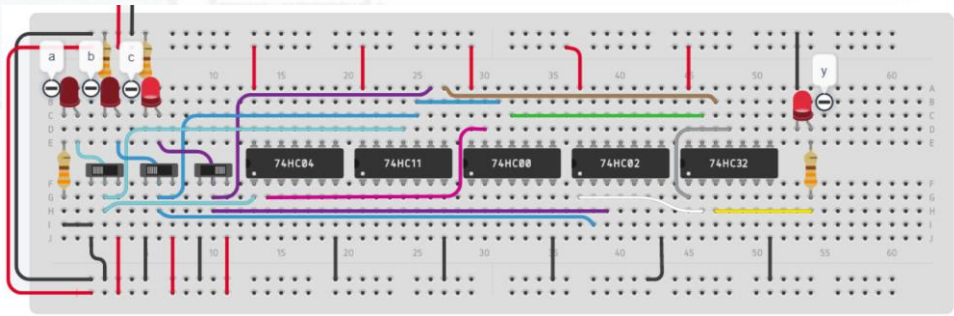


Revisão

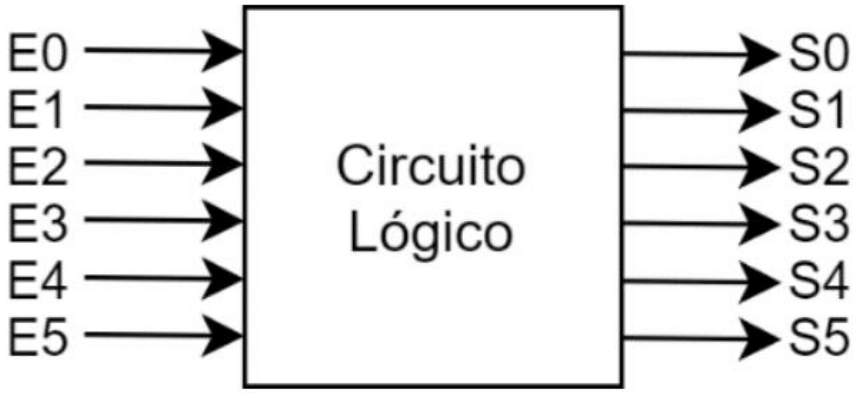
Porta	Símbolo	Função	Tabela Verdade	Circuito Integrado
Inversora (*NOT*)		$y = \bar{a}$	Entrada / Saída a / y 0 / 1 1 / 0	 7404
OU (*OR*)		$y = a + b$	a b y 0 0 0 0 1 1 1 0 1 1 1 1	 7432
E (*AND*)		$y = a \cdot b$	a b y 0 0 0 0 1 0 1 0 0 1 1 1	 7408
Não OU (*NOR*)		$y = \overline{a + b}$	a b y 0 0 1 0 1 0 1 0 0 1 1 0	 7402
Não E (*NAND*)		$y = \overline{a \cdot b}$	a b y 0 0 1 0 1 1 1 0 1 1 1 0	 7400
OU Exclusivo (XOR)		$y = a \oplus b$	a b y 0 0 0 0 1 1 1 0 1 1 1 0	 7486
Não OU Exclusivo (XNOR)		$y = \overline{a \oplus b}$	a b y 0 0 1 0 1 0 1 0 0 1 1 1	 74266

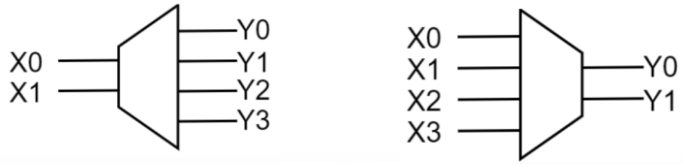


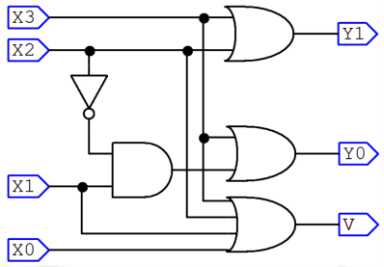


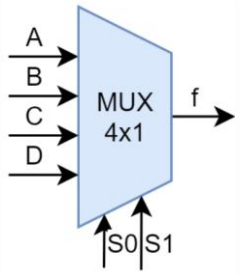


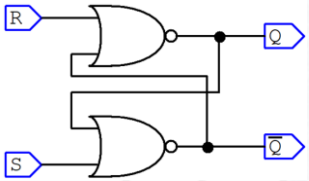
Revisão

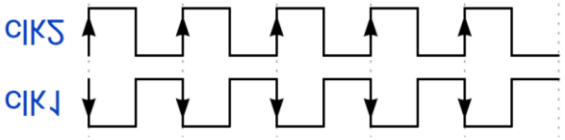

E0
E1
E2
E3
E4
E5
Circuito
Lógico
S0
S1
S2
S3
S4
S5

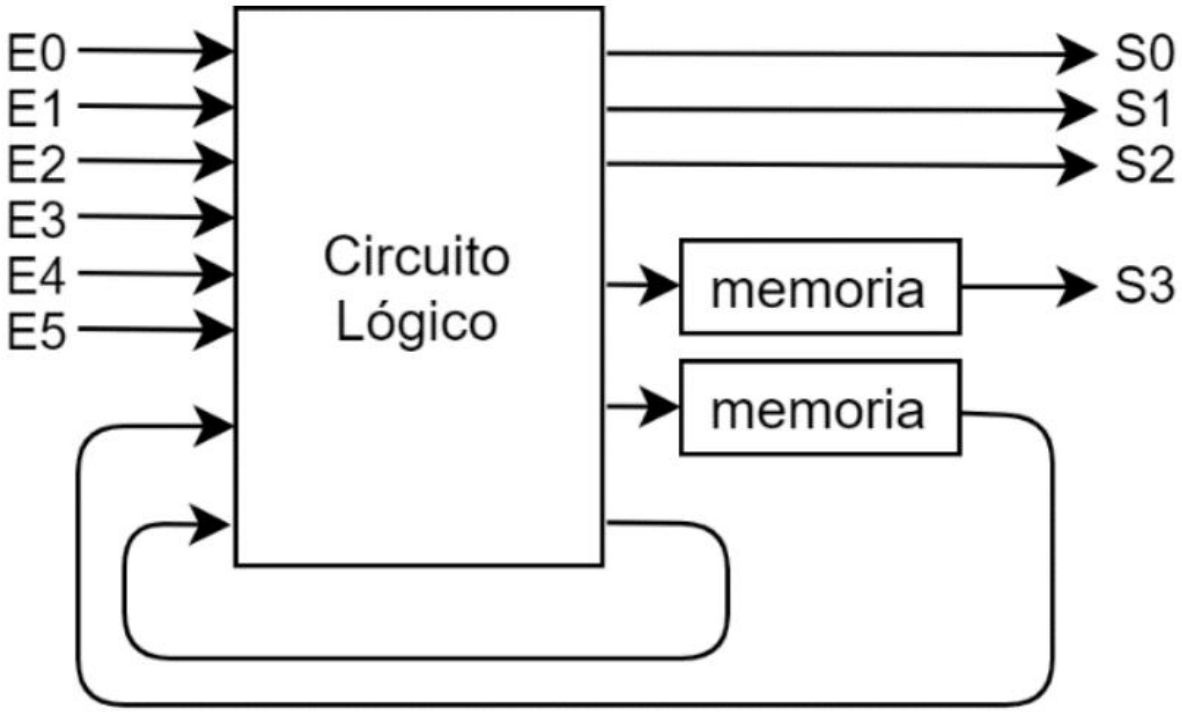

X0
X1
Y0
Y1
Y2
Y3
X0
X1
X2
X3
Y0
Y1

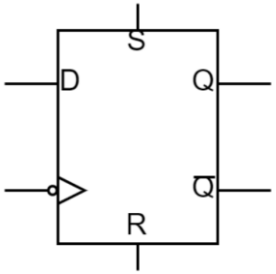

X3
X2
X1
X0
Y1
Y0
V

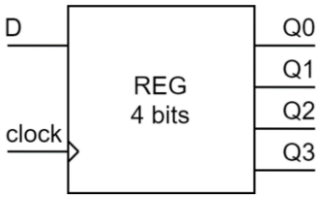

A
B
C
D
MUX
4x1
f
S0
S1


R
S
Q
Q̄

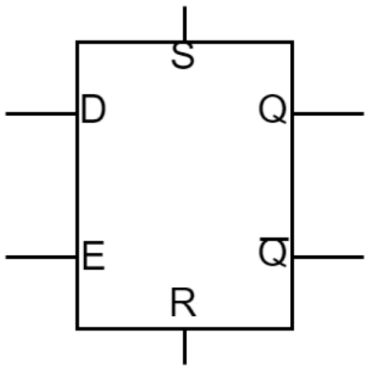

clk
clk

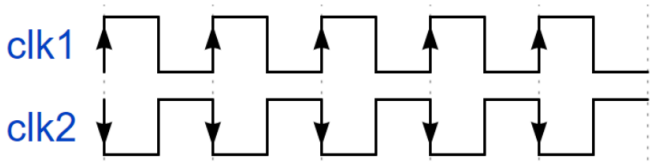

E0
E1
E2
E3
E4
E5
Circuito
Lógico
S0
S1
S2
memoria
S3
memoria


S
D
Q
Q̄
R

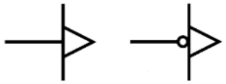

D
clock
REG
4 bits
Q0
Q1
Q2
Q3

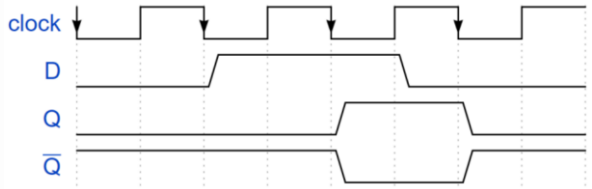
Revisão

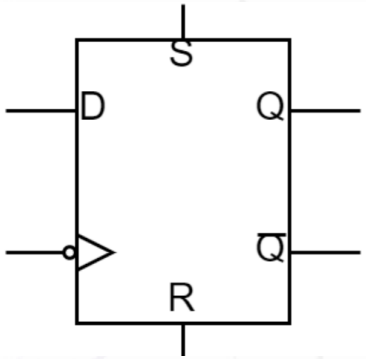


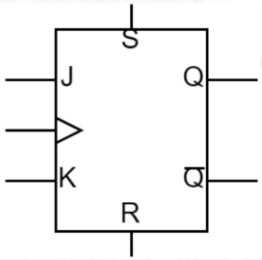


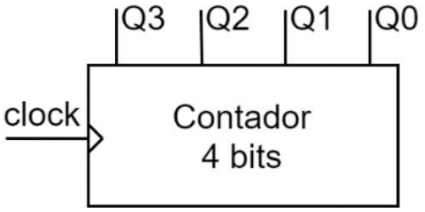
Entradas		Saídas	
clock	D	Q	$\bar{Q}$
0	X	Não muda	
1	X	Não muda	
↓	0	0	1
↓	1	1	0

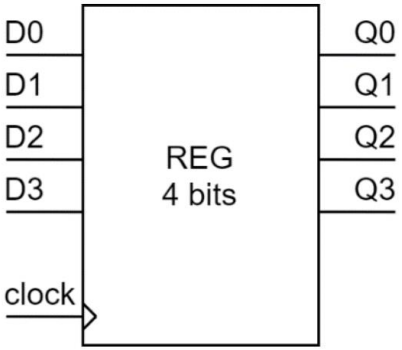


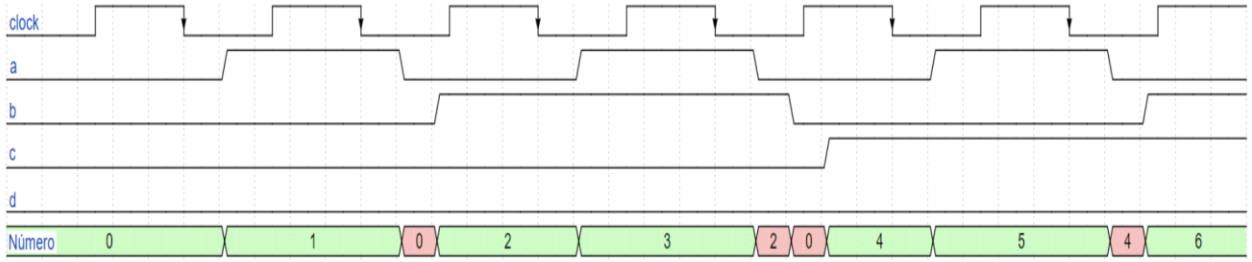


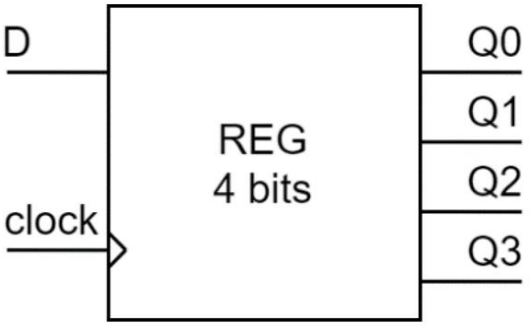




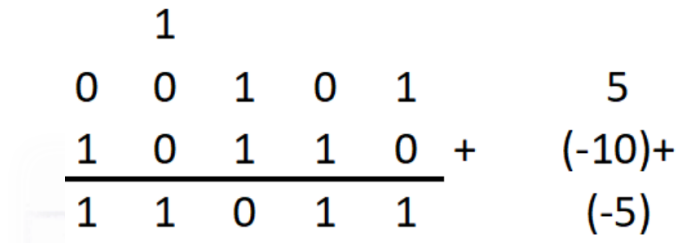


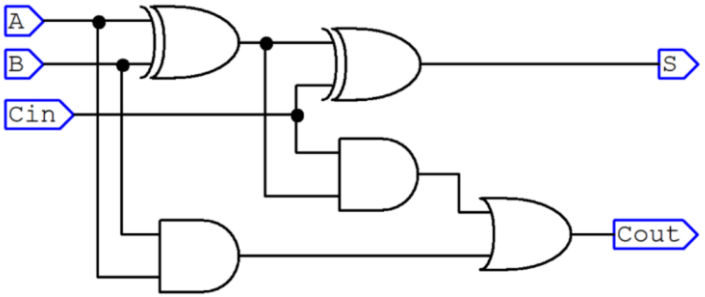


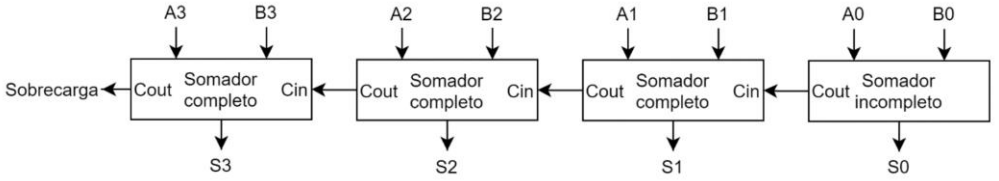


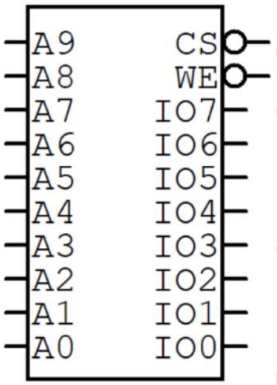


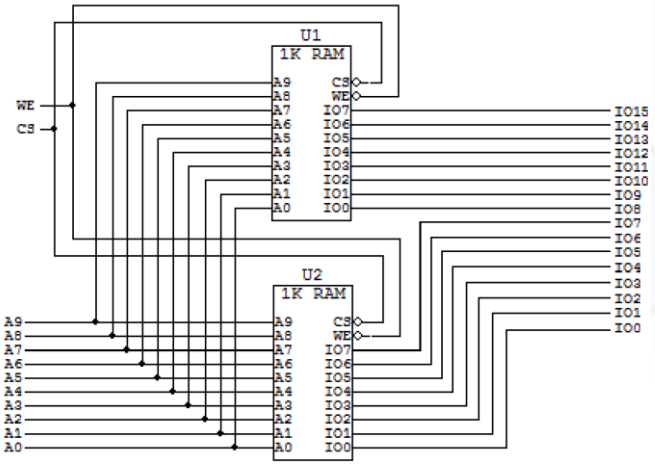
Revisão

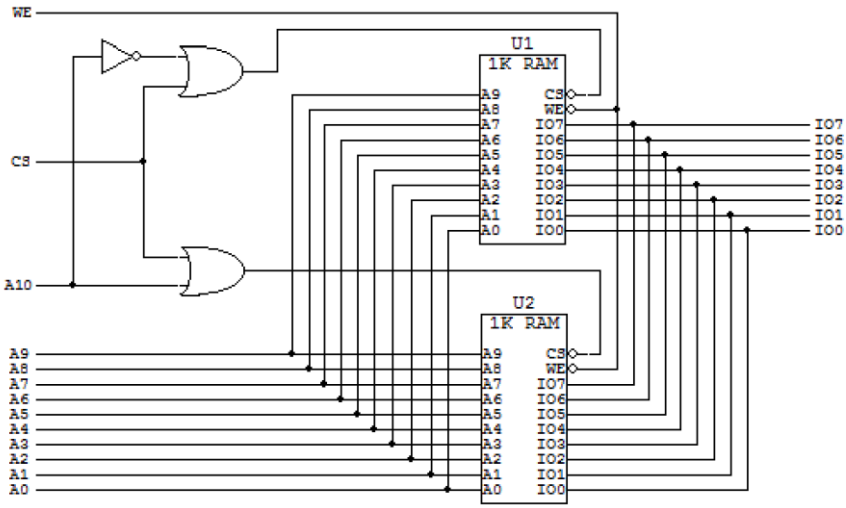

1
0 0 1 0 1 5
1 0 1 1 0 + (-10)+
1 1 0 1 1 (-5)

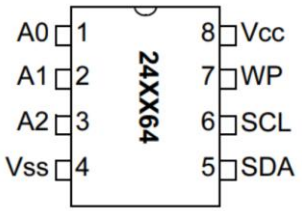

A
B
Cin
S
Cout


A3 B3 A2 B2 A1 B1 A0 B0
Sobrecarga
Cout Somador completo Cin
Cout Somador completo Cin
Cout Somador completo Cin
Cout Somador incompleto
S3 S2 S1 S0

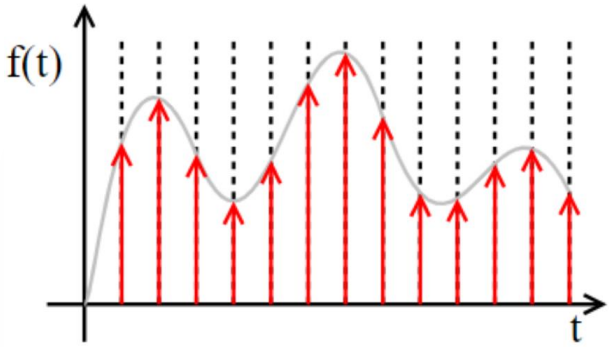

A9 CS
A8 WE
A7 IO7
A6 IO6
A5 IO5
A4 IO4
A3 IO3
A2 IO2
A1 IO1
A0 IO0

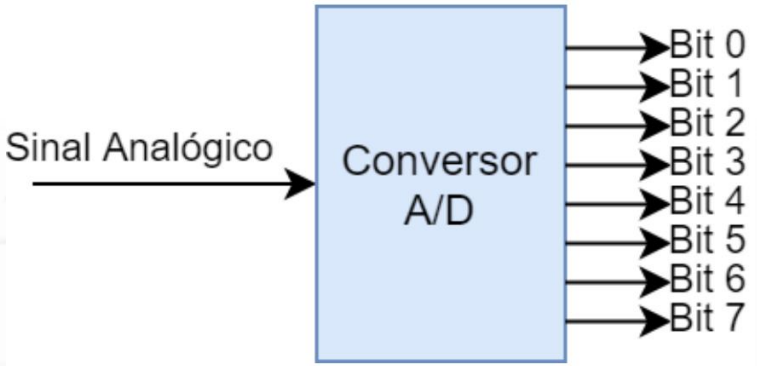

U1
1K RAM
U2
1K RAM
WE
CS
IO15 IO14 IO13 IO12 IO11 IO10 IO9 IO8 IO7 IO6 IO5 IO4 IO3 IO2 IO1 IO0

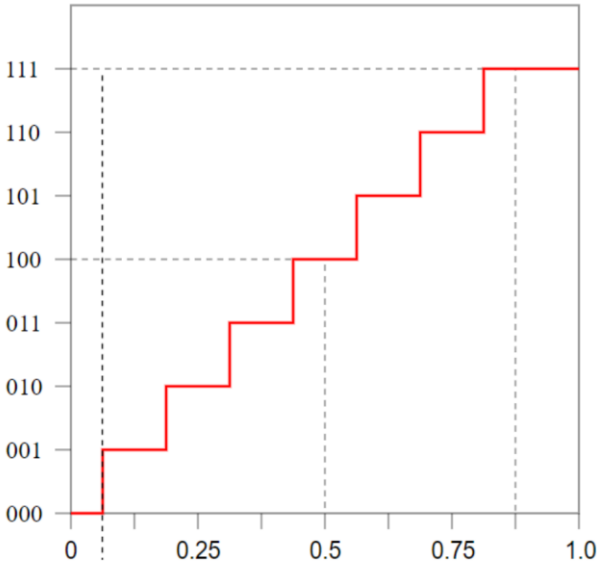

WE
CS
A10
U1
1K RAM
U2
1K RAM
IO7 IO6 IO5 IO4 IO3 IO2 IO1 IO0

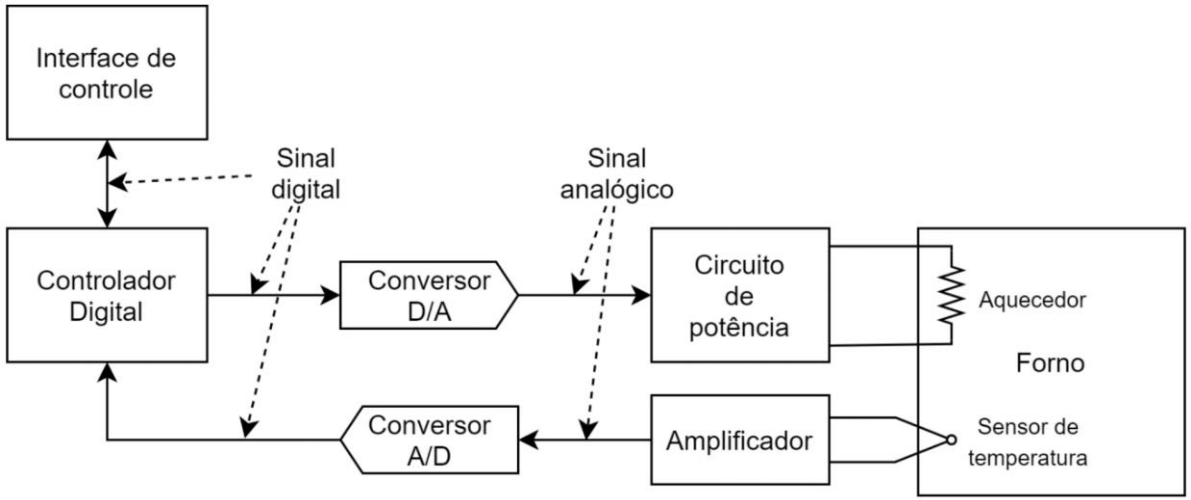

A0 1
A1 2
A2 3
Vss 4
24XX64
8 Vcc
7 WP
6 SCL
5 SDA

Revisão

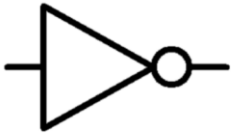

f(t)
t

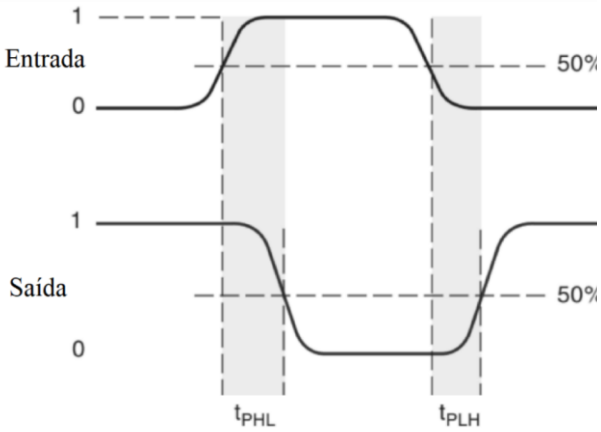

Sinal Analógico
Conversor
A/D
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7

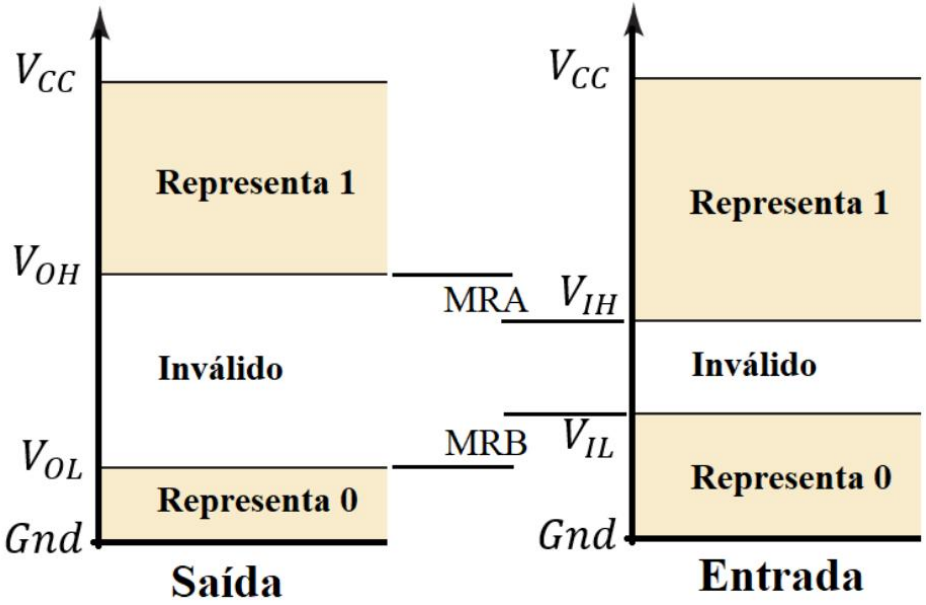

111
110
101
100
011
010
001
000
0
0.25
0.5
0.75
1.0

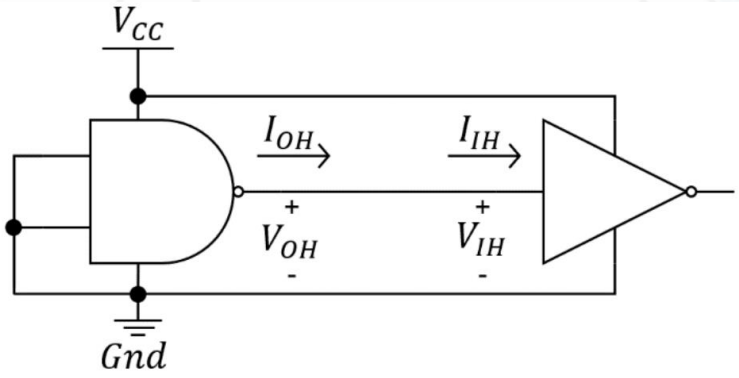

Interface de
controle
Sinal
digital
Sinal
analógico
Controlador
Digital
Conversor
D/A
Circuito
de
potência
Aquecedor
Forno
Conversor
A/D
Amplificador
Sensor de
temperatura

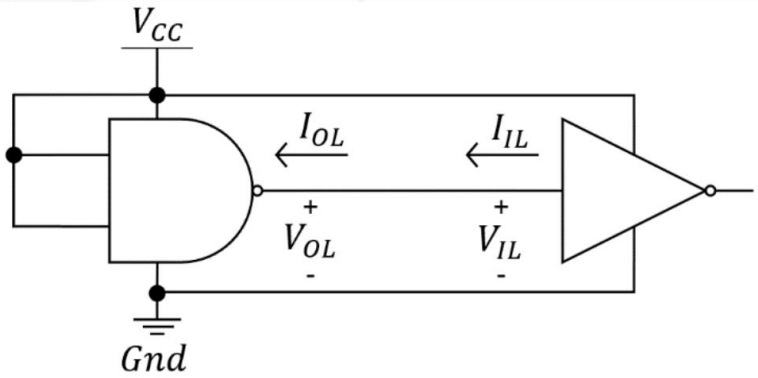
Revisão




1
Entrada
0
50%
1
Saída
0
50%
tPHL
tPLH

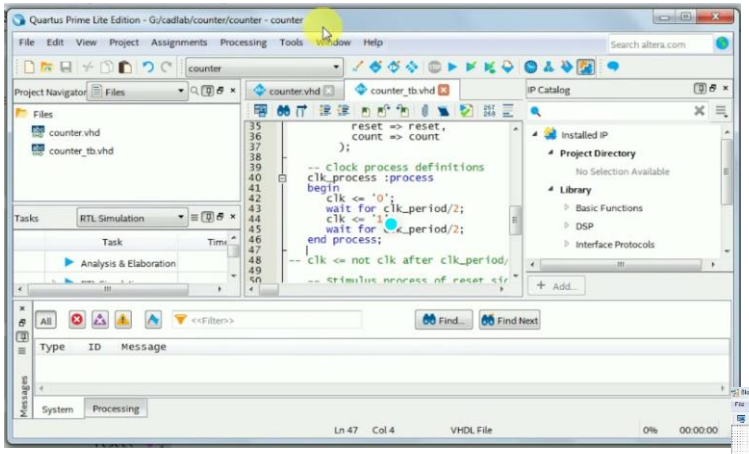

VCC
Representa 1
VOH
Inválido
VOL
Representa 0
Gnd
Saída
MRA
MRB
VCC
VIH
VIL
Representa 1
Inválido
Representa 0
Gnd
Entrada

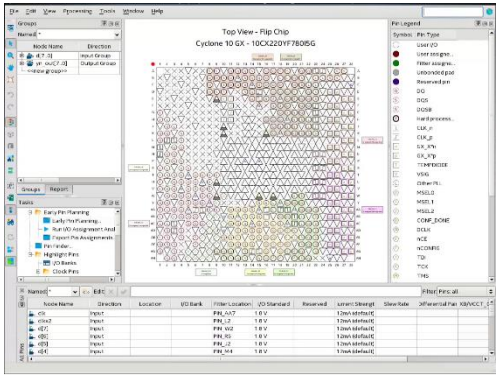

VCC
IOH
IIH
+
VOH
-
+
VIH
-
Gnd

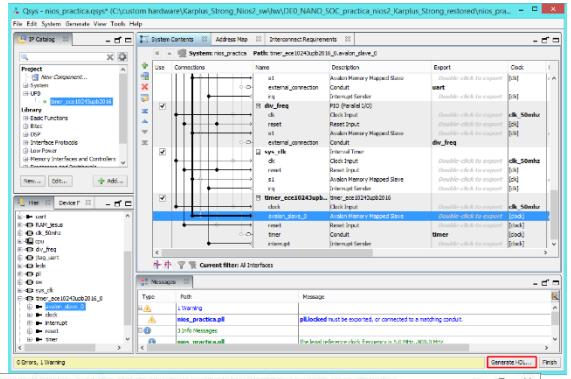

VCC
IOL
IIL
+
VOL
-
+
VIL
-
Gnd

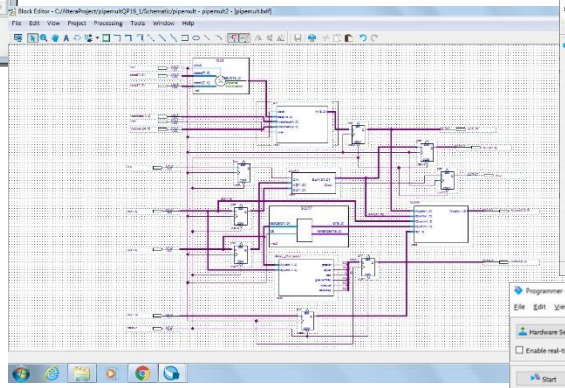
Ferramentas

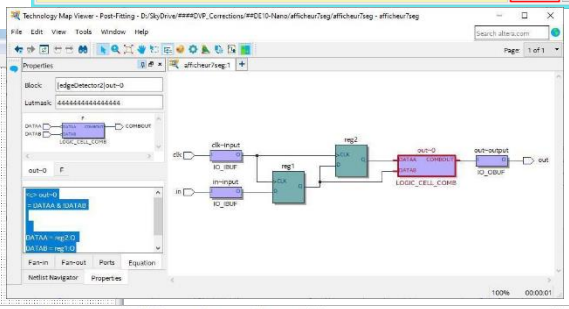
Intel Quartus Prime Lite

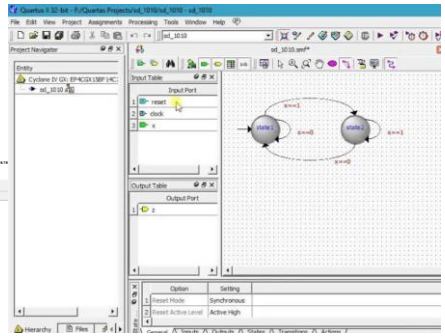


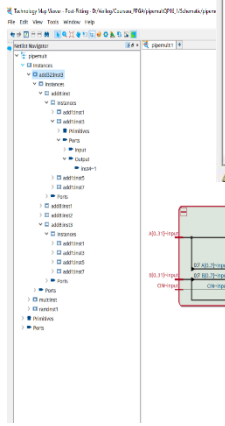


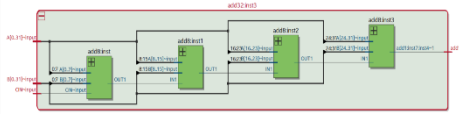


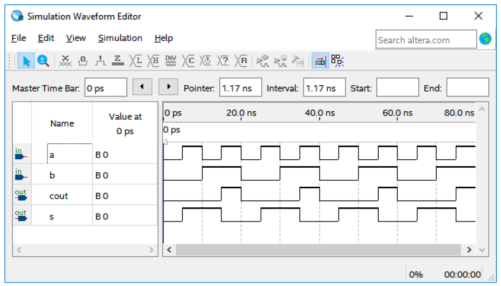












Ferramentas

Hneemann Digital